Bipolar Power Transistor
Data Book
1996

TEMIC

Semiconductors

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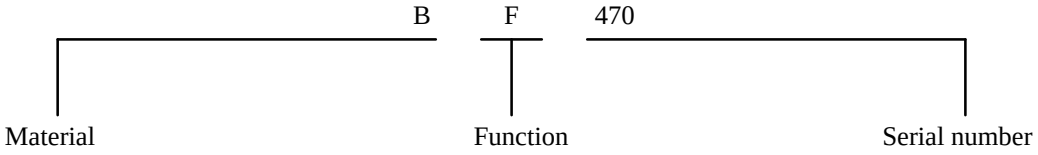
Conventions Used in Presenting Technical Data

Nomenclature for Semiconductor Devices According to Pro Electron

The part number of a semiconductor device consists two letters followed by a **serial number.**



The **first letter** indicates the material used for the active part of the device.

A GERMANIUM
(Materials with a band gap 0.6 – 1.0 eV) [1)]

B SILICON
(Materials with a band gap 1.0 – 1.3 eV) [1)]

C GALLIUM-ARSENIDE
(Materials with a band gap > 1.3 eV) [1)]

R COMPOUND MATERIALS
(For example Cadmium-Sulphide)

The **second letter** indicates the circuit function.

A DIODE: detection, switching or mixer

B DIODE: variable capacitance

C TRANSISTOR: low power, audio frequency

D TRANSISTOR: power, audio frequency

E DIODE: tunnel

F TRANSISTOR: low power, high frequency

G DIODE: oscillator and miscellaneous

H DIODE: magnetic sensitive

K HALL EFFECT DEVICE:
in an open magnetic circuit

L TRANSISTOR: power, high frequency

M HALL EFFECT DEVICE:
in a closed magnetic circuit

N PHOTO COUPLER

P DIODE: radiation sensitive

Q DIODE: radiation generating

R THYRISTOR: low power

S TRANSISTOR: low power, switching

T THYRISTOR: power

U TRANSISTOR: power, switching

X DIODE**:** multiplier, e.g., varactor, step recovery

Y DIODE: rectifying, booster

Z DIODE: voltage reference or voltage regulator, transient suppressor diode

The **serial number** consists of:

- A three-digit number from 100 to 999 for devices primarily intended for domestic equipment
- One letter (Z, Y, X etc.) and a two-digit number from 10 to 99, for devices primarily intended for professional equipment

A version letter can be used to indicate a deviation of a single characteristic, either electrical or mechanical. This letter never has a fixed meaning. The only exception is the use of the letter R, indicating reversed voltage (e.g., collector to case).

The code for semiconductors given above is used only for parts which are registered at **Pro Electron.** Some types have designation code (JEDEC):

1N two-digit to four-digit number indicates a diode

2N two-digit to four-digit number indicates a **transistor**

[1)] The material mentioned are examples

Polarity Conventions

The voltage direction is given

- by an arrow which points out from the measuring point to the reference point

or

- by a two-letter subscript, where the first letter is the measuring point and the second letter is the reference point.

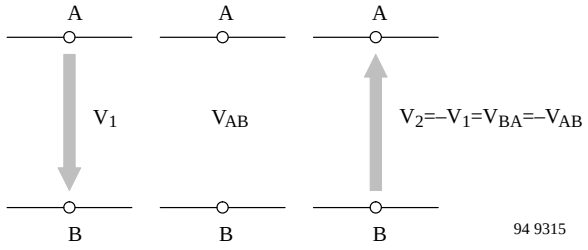


Figure 1.

The numerical value of the voltage is positive if the potential at the arrow tail is higher than at the arrow head; i.e., the potential difference from the measuring point (A) to the reference point (B) is positive.

The numerical value of the voltage is negative if the potential at the arrow tail is lower than at the arrow head; i.e., the potential difference from the measuring point to the reference point is negative.

In case of alternating voltages, once the voltage direction is selected, it is maintained throughout. The alternating character of the quantity is given with the time-dependent change in sign of its numerical values.

The current direction is shown with an arrow head drawn on the line (figure 2).

Figure 2.

The numerical value of the current is positive if the charge of the carriers moving in the direction of the arrow is positive (conventional current direction) or if the charge of the carriers moving against this direction is negative.

The numerical value of the current is negative if the charge of the carriers moving in the direction of the arrow is negative or if the charge of the carriers moving against this direction is positive.

The general rules stated above are also valid for alternating quantities. Once the direction is selected, it is maintained throughout. The alternating character of the quantity is given with the time dependent change in sign of its numerical values.

Polarity conventions for devices with three or more terminals

The following rules are valid:

Current arrows are always directed towards the device.

Voltage arrows are selected according to the basic configuration, i.e., the common electrode for the input and the output is chosen as the reference point.

Example: NPN transistor in common-emitter, common-base and common-collector configuration (figure 3)

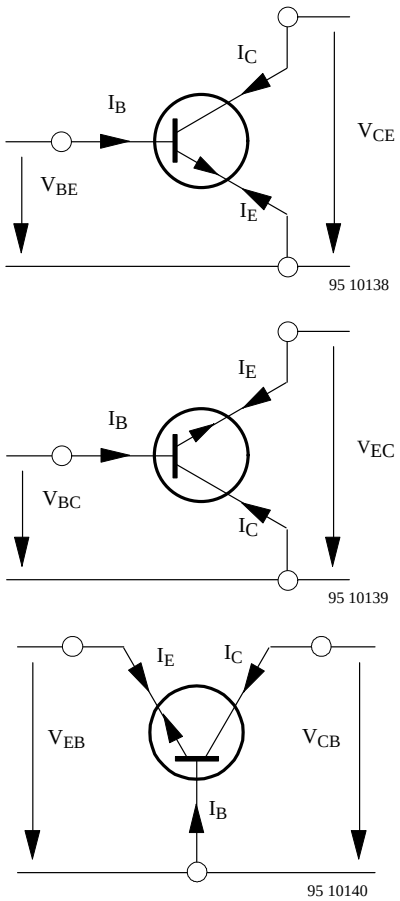


Figure 3.

Transistor Equivalent Circuit

Transistor characteristics can be explained with an equivalent circuit whose circuit elements (in contrast to four-pole coefficients) are considered constant over a wide frequency range. These parameters are highly bias- and temperature-dependent; therefore, the static conditions must be known completely.

The hybrid-π equivalent circuit developed by Giacolleto is a useful representation of certain transistor types because its parameters may be considered to be frequency-dependent (such as $f < 0.1\ f_T$).

With

$Y_{b'e} = g_{b'e} + j \times \omega \times C_{b'e}$

$Y_{b'c} = g_{b'c} + j \times \omega \times C_{b'c}$

$Y_{ce} = g_{ce} + j \times \omega \times C_{ce}$

and

$A = 1 + (Y_{b'e} + Y_{b'c})\, r_{bb'}$

it is possible to obtain the y-parameters (admittance coefficients) in common emitter configuration:

$$Y_{ie} = Y_{11e} = \frac{1}{A}(Y_{b'e} + Y_{b'c})$$

$$Y_{re} = Y_{12e} = -\frac{1}{A} \times Y_{b'c}$$

$$Y_{fe} = Y_{21e} = \frac{1}{A}(g_m - Y_{b'c})$$

$$Y_{oe} = Y_{22e} = \frac{1}{A} \times r_{bb'} \times Y_{b'c}\,(g_m - Y_{b'c}) + Y_{b'c} + Y_{ce}$$

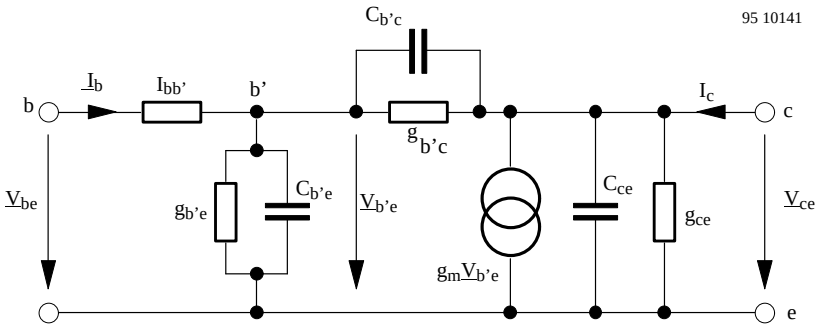


Figure 4.

Arrangement of Symbols

Letter symbols for current, voltage and power (according to DIN 41 875, sheet 1)

A system of basic letter symbols is used to represent current voltage and power. Capital letters are used for the representation of peak, mean, dc or root-mean-square values. Lower case letters are used for the representation of instantaneous values which vary with time.

As subscripts, capital letters are used to represent continuous or total values while lower case letters are used to represent the varying values. Table 1 summarizes the rules given above.

Table 1.

Basic Letter	
Lower Case	Upper Case
Instantaneous values which vary with time	Maximum (peak), average (mean) continuous (dc) or root-mean-square (RMS) values

Subscript(s)	
Lower Case	Upper Case
Varying component alone, i.e., instantaneous, root-mean-square, maximum or average values	Continuous (without signal) or total (instantaneous, average or maximum) values

Letter symbols for impedance, admittances, four-pole parameters etc.

For impedance, admittance, four-pole parameters etc., upper case letters are used for the representation of external circuits and of circuits in which the device is only a part. Lower case letters are used for the representation of electrical parameters inherent in the device.

These rules are not valid for inductance and capacitance. Both these quantities are denoted with capital letters.

As subscripts, upper case letters are used for the designation of static (dc) values, while lower case letters are used for the designation of small-signal values.

If more than one subscript is used (h_{FE}, h_{fe}), the letter symbols are either all upper case or all lower case.

If the subscript has numeric (single, double, etc.) as well as letter symbol(s) (such as h_{21E}, or h_{21e}), the differentiation between static and small-signal value is made only by subscript letter symbols.

Other quantities (values) which deviate from the rules above are given in the list of letter symbols.

Table 2 summarizes the application of the rules given above.

Table 2.

Basic Letter	
Lower Case	Upper Case
Electrical parameters inherent in the semiconductor devices except inductance and capacitance	Electrical parameters of external circuits and of circuits in which the semiconductor device forms only a part; all inductance and capacitance

Subscript(s)	
Lower Case	Upper Case
Small-signal values	Static (dc) values

Examples:

R_G
Generator resistance

G_p
Power gain

h_{FE}
DC forward current transfer ratio in common emitter configuration

r_p
Parallel resistance, damping resistance

Example to Use Symbols According to DIN 41 785 and IEC 148

a) Transistor

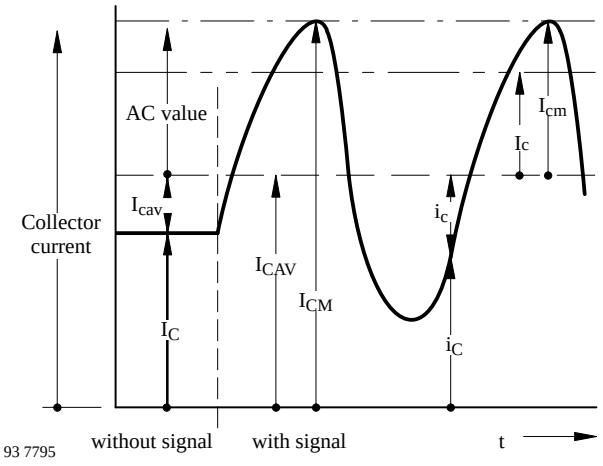


Figure 5.

I_C	dc value, no signal
I_{CAV}	Average total value
I_{CM};I_C	Maximum total value
I_{CEFF}	RMS total value
I_C;I_{CEFF}	RMS varying component
I_{CM};I_C	Maximum varying component value
i_C	Instantaneous total value
i_C	Instantaneous varying component value

The following relationships are valid:

$I_{CM} = I_{CAV} + I_{cm}$

$i_C = I_{CAV} + i_c$

b) Diode

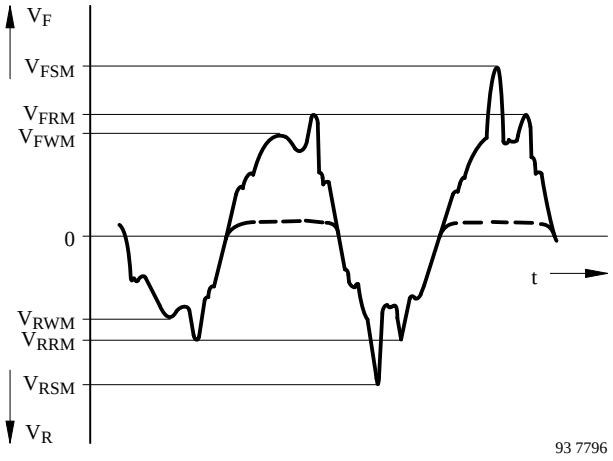


Figure 6.

V_F	Forward voltage
V_R	Reverse voltage
V_{FSM}	Surge forward voltage (non-repetitive)
V_{RSM}	Surge reverse voltage (non-repetitive)
V_{FRM}	Repetitive peak forward voltage
V_{RRM}	Repetitive peak reverse voltage
V_{FWM}	Crest working forward voltage
V_{RWM}	Crest working reverse voltage

Symbols and Terminology

AQL
Acceptable Quality Level (see chapter ‘Quality Data’)

B, b
Base, base terminal

C, c
Collector, collector terminal

C
Capacitances

The transistor equivalent circuit (see chapter ‘Transistor Equivalent Circuit’) shows the different capacitances in a transistor. In addition, there are capacitances between terminals, inside as well as outside the case. All these capacitances play an active role, first at high frequencies. Here, the actual operating capacitances are important, but not the equivalent circuit capacitances. They can be explained best with y-coefficients.

C_i
Short-circuit input capacitance $C_{11} = C_i$
An imaginary part of short-circuit input admittance y_{11} (= y_i) divided by a factor $j \times \omega$
The values of capacitances are circuit-configuration dependent; therefore, a further subscript e, b or c is added to designate the orientation.

C_{ib}
Short-circuit input capacitance in common-base configuration

$$C_{11b} = C_{ib} = \frac{1}{j\omega} \times \mathrm{Im}\ (y_{ib})$$

C_{ie}
Short-circuit input capacitance in common-emitter configuration

$$C_{11e} = C_{ie} = \frac{1}{j\omega} \times \mathrm{Im}\ (y_{ie})$$

C_{issg1}
Gate 1 input capacitance in common-source configuration

C_{issg2}
Gate 2 input capacitance in common-source configuration.
An imaginary part of short-circuit output admittance $y_{22} = y_O$, divided by a factor ($j \times \omega$), $C_{22} = C_O$

C_o
Short-circuit output capacitance

C_{ob}
Short-circuit output capacitance in common-base configuration

$$C_{22b} = C_{ob} = \frac{1}{j\omega} \times \mathrm{Im}\ (y_{ob})$$

C_{oe}
Short-circuit output capacitance in common-emitter configuration

$$C_{22e} = C_{oe} = \frac{1}{j\omega} \times \mathrm{Im}\ (y_{oe})$$

C_{oss}
Output capacitance in common-source configuration

C_{rss}
Feedback capacitance in common-source configuration

$C_{ür}$
Short-circuit reverse transfer capacitance
An imaginary part of short-circuit reverse transfer admittance $y_{21} = y_r$, divided by a factor ($-j\omega$), $C_{ür} = -C_{12} = -C_r$

$C_{ürb}$
Feedback capacitance in common-base configuration (= $-C_{rb}$)

$$-C_{12b} = C_{ürb} = \frac{1}{j\omega} \times \mathrm{Im}\ (y_{rb})$$

$C_{üre}$
Feedback capacitance in common-emitter configuration (= $-C_{re}$)

$$-C_{12e} = C_{üre} = \frac{1}{j\omega} \times \mathrm{Im}\ (y_{re})$$

There are additional **capacitances** given in data sheets. These are the result of direct measurements given below.

C_{CB}
Capacitance between collector and base without parasitic capacitances

C_{CBO}
Capacitance between collector and base with open emitter
It can be measured by applying reverse bias to its terminals.

The following relationship is also valid:

$$C_{CBO} \approx C_{oe} \approx C_{ob}$$

(Different configurations, but approximately the same values)

C_{EB}
Capacitance between emitter and base without parasitic capacitances

C_{EBO}
Capacitance between emitter and base with an open collector
Measurement is made by applying reverse bias to its terminals.

The following relationship is also valid:

$C_{EBO} \approx C_{ie} \approx C_{ib}$

(Different configurations, but approximately the same values)

C_p
Parallel capacitance, case capacitance

E, e
Emitter

E_L
Inductive energy

f
Frequency

f_g
Cut-off frequency

f_{hfe}
h_{fe} cut-off frequency (β cut-off frequency, f_β)

The frequency at which the modulus of current amplification factor (h_{fe}) has decreased to 0.707 times of its low frequency (1 kHz) value.

f_T
Gain bandwidth product, transition frequency

The product of the modulus of the common-emitter small-signal short-circuit forward current transfer ratio, and the frequency of measurement f_M
This frequency is chosen such that h_{fe} is decreasing at a slope of approximately 6 dB per octave. The associated angular frequency $\omega_T = 2 \times n \times f_T$ is defined as the reciprocal value of transit time minority carriers through the base region.

g_i
Short-circuit input conductance

g_{ib}
Input conductance in common-base configuration, short circuit at output g_{ib} = RE (y_{ib})

g_{ie}
Input conductance in common-emitter configuration, short circuit at output g_{ie} = Re (y_{ie})

g_o
Short-circuit output conductance

g_{ob}
Output conductance in common-base configuration, short circuit at input g_{ob} = Re (y_{ob})

g_{oe}
Output conductance in common-emitter configuration short circuit at input g_{oe} = Re (y_{oe})

G_{pb}
Power gain in common-base configuration

G_{pe}
Power gain in common-emitter configuration

g_r
Short-circuit reverse conductance

G_v
Unilateral gain

h_{FE}
DC forward current transfer ratio in common emitter configuration

It is the ratio of the collector current, I_C, to the base current, I_B, for specified values of V_{CE} and I_C

It is also denoted by the letter B.

h_{fe}
Short-circuit forward current transfer ratio in common emitter configuration (small-signal value)

h_{fe} is the ratio of the alternating collector current, i_c, to the alterning base current, i_b, for small signals with output being short circuited to ac.

It is also known as β.

In technical data sheets, this parameter is given with a 1 kHz sine wave for a specified operating point. This quantity is also known as current amplification factor.

I_B
DC base current

I_{BM}
Peak base current

I_C
DC collector current

I_{CBO}
Collector cut-off current with open emitter

Cut-off current is the reverse current which flows through the junction(s) (base-emitter or base-collector) of a transistor when reverse bias is applied across its terminals, the third terminal being open-circuited or otherwise specified. It is also known as leakage current.

Collector-base cut-off current, I_{CBO}, and collector-base V_{CBO}, with open emitter, i.e., $I_E = 0$ A

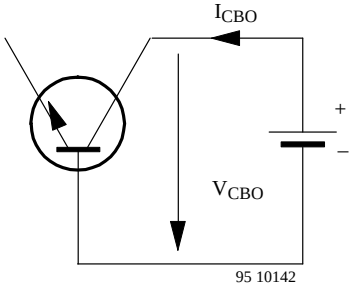


Figure 7.

I_{CEO}
Collector cut-off current, with open base

Collector-emitter cut-off current, I_{CEO}, and collector-emitter voltage, V_{CEO}, with open base (i.e., $I_B = 0$ A)

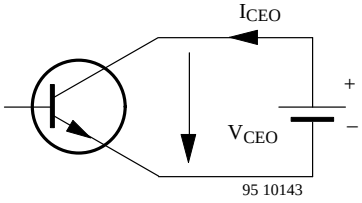


Figure 8.

I_{CER}
Collector cut-off current with a resistor R_{BE} connected between base and emitter

Collector-emitter cut-off current, $I_{CER,}$ and collector-emitter voltage, V_{CER}, having resistance connected between base and emitter. The appropriate value of $R_{BE,}$ referring to V_{CER} and $I_{CER,}$ is also given in the technical data sheet. For higher values of $R_{BE,}$ the values of V_{CEO} and I_{CEO} are valid.

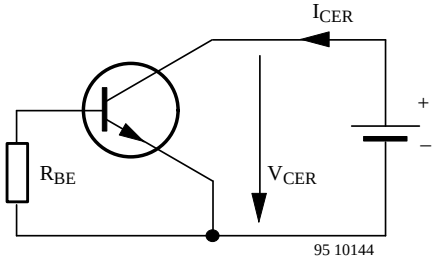


Figure 9.

I_{CES}
Collector cut-off current, short circuit between base and emitter

Collector cut-off current, $I_{CES} = I_{CBS}$, and collector emitter voltage, $V_{CES} = V_{CBS}$, with base emitter short circuited

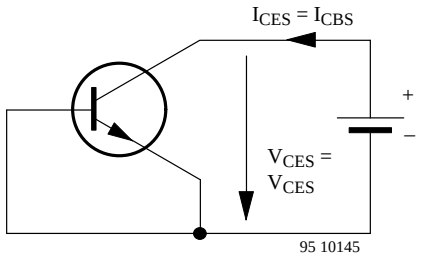


Figure 10.

I_{CEV}
Collector cut-off current with reverse base-emitter voltage

Collector-emitter cut-off current, I_{CEV}, and collector-emitter voltage, V_{CEV}, when the applied voltage between base and emitter is reverse biased

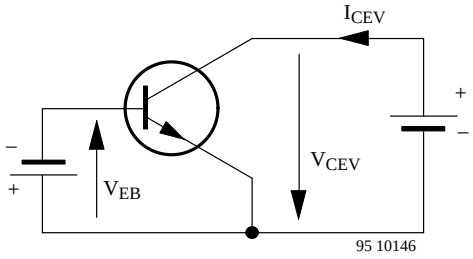


Figure 11.

I_{CEX}
Collector cut-off current with forward base-emitter voltage

Collector-emitter cut-off current, $I_{CEX,}$ when the applied voltage between base and emitter is forward biased

The value of the base-emitter voltage, V_{BE}, is selected such that no appreciable base current flows.

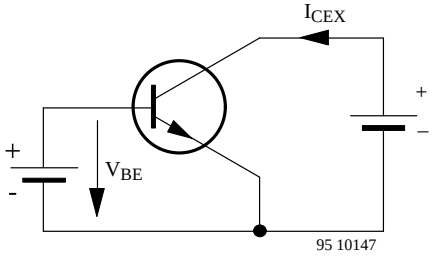


Figure 12.

I_{CM}
DC collector peak current

I_{CM} is the maximum collector current with a sine wave operation, $f \geq 25$ Hz, or pulse operation, $f \geq 25$ Hz, having duty cycle $t_p/T \leq 0.5$.

I_E
Emitter current

I_{EBO}
Emitter cut-off current with open collector

Emitter-base cut-off current, I_{EBO}, and emitter-base voltage, V_{EBO}, with open collector, i.e., $I_C = 0$ A

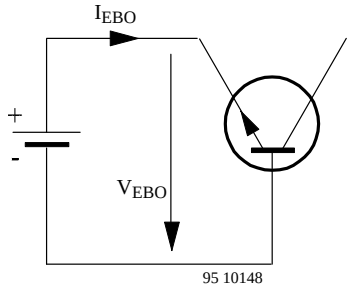


Figure 13.

I_I
Input current

I_K
Short-circuit current

I_Q
Output current

I_S
Supply current

K
Kelvin

l
Length, connecting lead length

L_s
Series inductance

M_A
Tightening torque

P
Power

P_I
Input power

P_q, P_Q
Output power

P_{tot}
Total power dissipation

P_{tot} is the dispersion of the heat generated within a device when a current flows through it. The allowable power dissipation, $P_{tot\ max}$, which is specified under absolute maximum ratings, is a function of T_{jmax}, T_{amb}, R_{thJA} and R_{thJC} given as follows:

$$P_{tot\ max}\ (amb) = \frac{T_{jmax} - T_{amb}}{R_{thJA}}$$

or

$$P_{tot\ max}\ (case) = \frac{T_{jmax} - T_{case}}{R_{thJC}}$$

In addition, power dissipation is limited in certain cases through safe operating areas given in data sheet.

P_v
Power dissipation, general

r_{bb}
Basic intrinsic resistance

R_{BE}
Resistance connected between base and emitter

r_F
DC forward resistance

r_f
Differential forward resistance

R_G
Generator resistance

r_i
Input resistance

R_L
Load resistance

r_p
Parallel resistance, damping resistance

r_q
Output resistance

R_{thJA}
Thermal resistance, junction ambient

R_{thJC}
Thermal resistance, junction case

T
Period

T
Absolute temperature, Kelvin temperature
0 K = –273.15°C, unit: K (Kelvin)

t
Time

T
Temperature, measured in centigrade, unit: °C (Celsius)

T_{amb}
Ambient temperature

If self-heating is significant, T_{amb} is the temperature of the surrounding air below the device under conditions of thermal equilibrium.

If self-heating is not significant, T_{amb} is the air temperature in the immediate surroundings of the device.

T_{amb}
Ambient temperature range

As an absolute maximum rating, T_{amb} is the maximum permissible ambient temperature range.

T_{case}
Case temperature

The temperature measured at a specified point on the case of a semiconductor device
Unless otherwise stated, this temperature is given as the temperature of the mounting base for transistors with metal can.

t_d
Delay time, see chapter ‘Switching Characteristics’

t_f
Fall time, see ‘Switching Characteristics’

t_{fr}
Forward recovery time

T_j
Junction temperature

The spatial mean temperature which the junction has acquired during operation
In the case of the transistors, it is mainly the temperature of the collector junction because its inherent temperature is maximum.

T_K
Temperature coefficient

The ratio of the relative change of an electrical quantity to the change in temperature (Δt) which causes it under otherwise constant operating conditions

T_L
Connecting lead temperature in holder at a distance, I, from case

t_{off}
Turn-off time, see chapter ‘Switching Characteristics’

t_{on}
Turn-on time, see chapter ‘Switching Characteristics’

t_p
Pulse duration

$\frac{t_p}{T}$

Duty cycle

t_r
Rise time, see chapter ‘Switching Characteristics’

t_{rr}
Reverse recovery time

t_s
Storage time, see chapter ‘Switching Characteristics’

T_{sd}
Soldering temperature

Maximum allowable temperature for soldering with specified distance from case and its duration, see chapter ‘Soldering Instructions’

T_{stg}
Storage temperature range

The temperature range at which the device may be stored or transported without any applied voltage

V_{BB}
Base-supply voltage

V_{BE}
Base-emitter voltage

V_{BEsat}
Base-saturation voltage

The base-emitter saturation voltage, V_{BEsat}, is the base-emitter voltage which belongs to the collector-emitter saturation voltage V_{CEsat}.

$V_{(BR)}$
Breakdown voltage

Reverse voltage at which an increase in voltage results in a sharp rise of reverse current
Breakdown voltage is given in technical data sheets for a specified current.

$V_{(BR)CBO}$
Breakdown voltage, collector-base, open emitter

$V_{(BR)CEO}$
Breakdown voltage, collector-emitter, open base

Measurements with pulsed current-collector source

The test circuit shown in figure 14 is connected to a switched-off inductive load. It is set in breakdown position until the storage energy during switch-on has been discharged; that is, until the ramp-shaped pulse current inflow at the collector has reached its zero value.

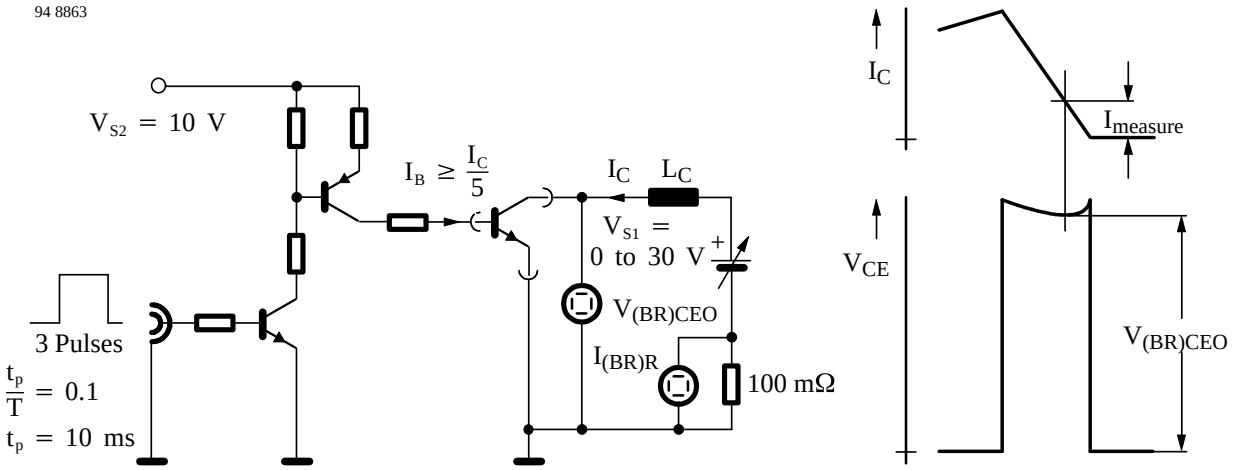


Figure 14.

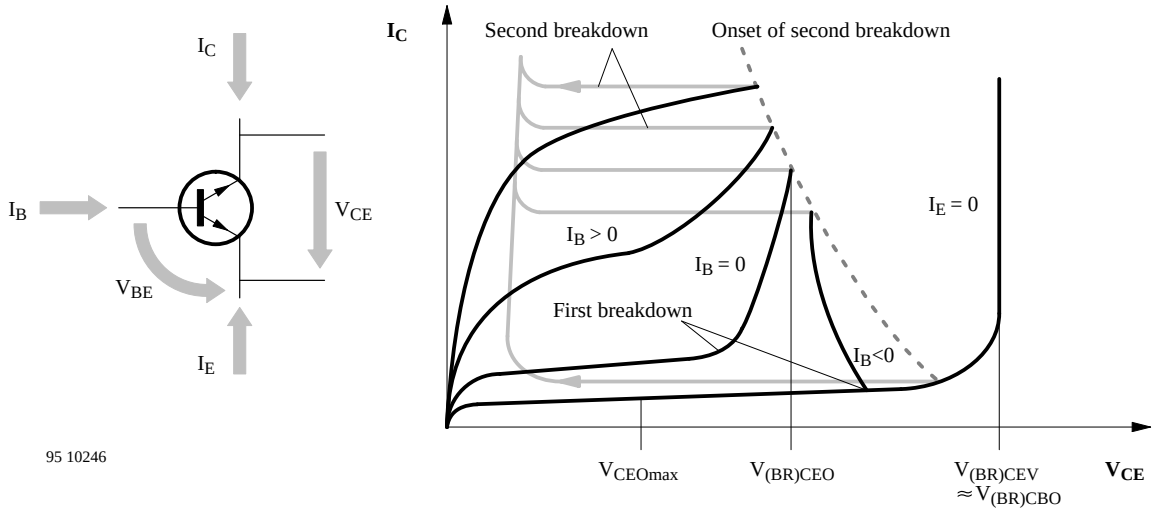


Figure 15. Typical voltage breakdown behaviour of a power transistor

Absolute maximum ratings of $V_{(BR)CEO}$ are defined with the test current, I_{test}, where the transistor has its lowest breakdown voltage value.

Breakdown voltage and collector inductance are dimensioned in such a way that the load of breakdown energy is below the value of transistor failure.

$V_{(BR)CEV}$
Collector-emitter breakdown voltage at a defined reverse voltage between base and emitter

$V_{(BR)EBO}$
Breakdown voltage, emitter-base, open collector

$V_{(BR)ECO}$
Breakdown voltage, emitter-collector, open base

V_{CB}
Collector-base voltage

V_{CBO}
Collector-base voltage, open emitter

Generally, reverse biasing is the voltage applied to any of two terminals of a transistor in such a way that one of the junction operates in reverse direction, and the third terminal (second junction) is specified separately.

V_{CC}
Collector-supply voltage

V_{CE}
Collector-emitter voltage

V_{CEO}
Collector-emitter voltage, open base

V_{CER}
Collector-emitter voltage with a resistor R_{BE} connected between base and emitter

V_{CES}
Collector-emitter voltage, short circuit between base and emitter

V_{CEsat}
Saturation voltage, collector-emitter

The collector saturation voltage is the dc voltage between the collector and emitter for specified saturation conditions.

Saturation voltage V_{CEsat} is given:

a) for a specified value of I_C, where the base-emitter voltage equals the collector-emitter voltage, i.e., V_{CB} = 0 V

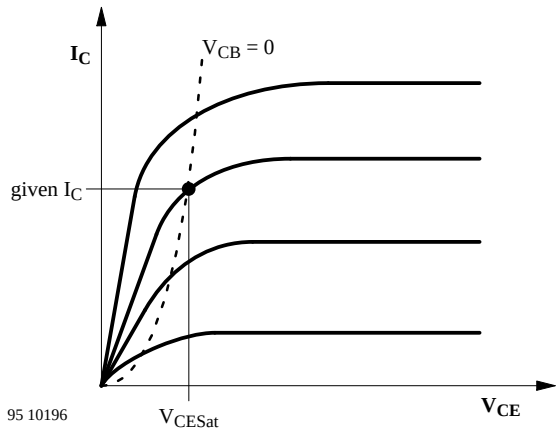


Figure 16.

b) for a specified value of I_C and I_B, where the operating point lies in the saturation region, i.e., $V_{CE} < V_{CB}$

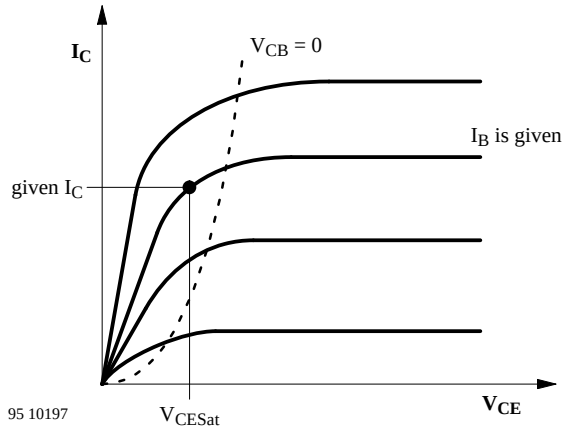


Figure 17.

c) for a specified value of I_C on the characteristic curve (I_B is constant) which intersects the curve point $I_C' = K\ I_c$ (K = 1.1) and a specified value of collector-emitter voltage (V_{CE} = 1 V)

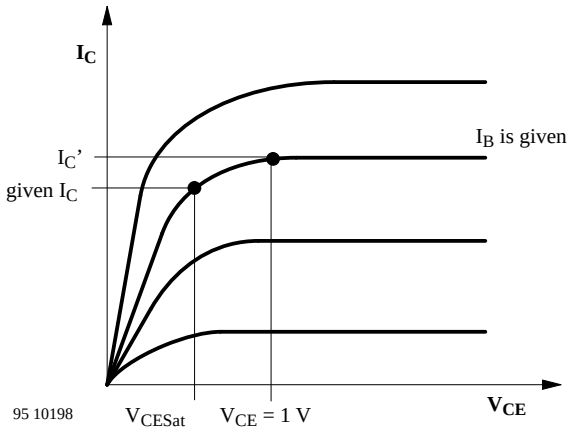


Figure 18.

$V_{CEsatHF}$
Collector-emitter HF saturation voltage

V_{CEV}
Collector-emitter voltage, with reverse base-emitter voltage

V_{EBO}
Emitter-base voltage, with open collector

V_R
Reverse voltage

Voltage drop which results from the flow of reverse current.

An external voltage applied to a semiconductor PN or NP junction to reduce the flow of current across the junction and thereby widen the depletion region

V_s
Supply voltage

V_T
Voltage due to temperature

Z_{thP}
Thermal impedance, pulse load
To determine the maximum power dissipation, $P_{tot\,max}$, of a transistor by repetitive rectangular pulse operation, calculation is as follows:

$$P_{totM} = \frac{T_{jM} - T_{case}}{Z_{thP}}$$

where

$T_{jmax} \triangleq t_{jM} =$

maximum (crest) allowable crystal temperature by repetitive pulse operation,

$$P_{totM} = \frac{T_{jmax} - T_{case}}{Z_{thP}}$$

Z_{thP} = thermal impedance, pulse operation,

$\frac{t_p}{T}$ as a parameter

Calculated, $P_{tot\,max}$ should correspond with the maximum allowable operating range as shown in figure 19.

π

Efficiency

τ_s
Storage time constant

■
New type

●●
Available as quality-tested device

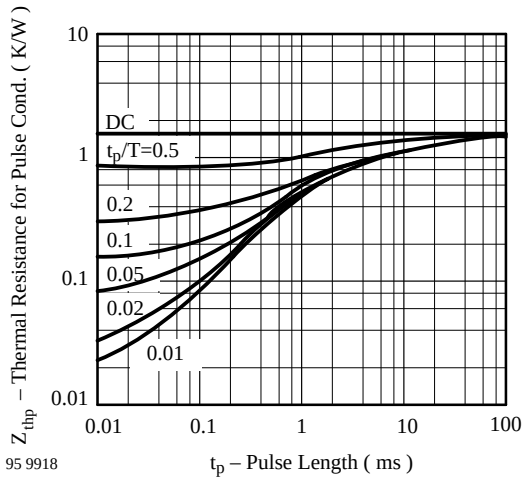


Figure 19.

Switching Characteristics

By using a transistor as a switch, it has to be kept in mind that in the transition from off-state to on-state the signal does not respond instantaneously even with abrupt changes in control values. The output signal is not only delayed but also distorted. These switching characteristics are explained by looking at an NPN transistor.

Figure 20 shows the basic circuit.

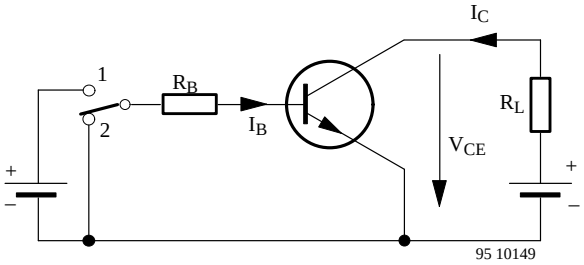


Figure 20.

The input (i.e., base current, i_B) and output (i.e., collector current, i_C) signals, are shown in figure 21.

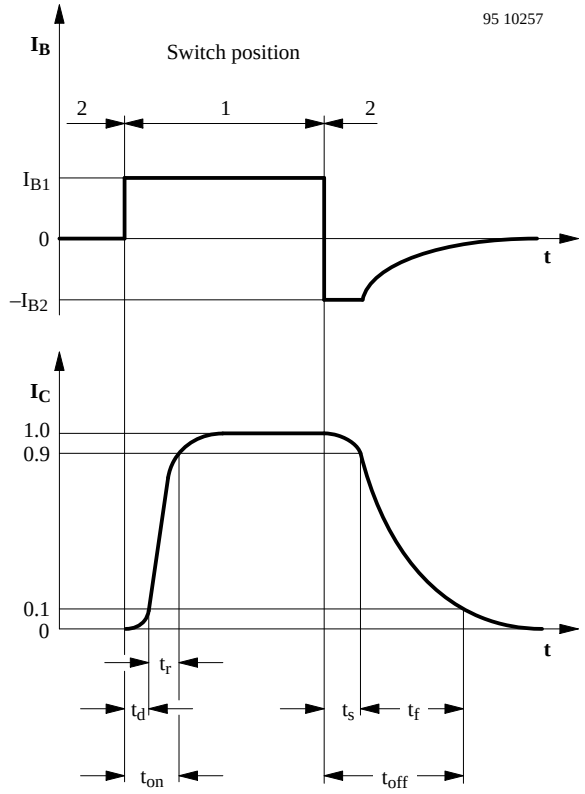


Figure 21.

The transient responses as shown in figure 20 with respect to figure 19 are given as follows:

t_d	delay time
t_r	rise time
t_{on} ($t_d + t_r$)	turn-on time
t_s	storage time
t_f	fall time
t_{off} ($t_s + t_f$)	turn-off time

These switching characteristics depend on the transistor type and the circuit used. They are only valid if the slope of the control pulse is much greater than that of collector current pulse. If the saturation factor is higher, turn-on time is shorter, and turn-off time is longer. Turn-off time is shorter if the on-off base current ratio is higher.

On-off base current ratio, a, is the ratio between the turn-off base current, I_{B2}, to the base current,

$$I_{B0} = \frac{I_C}{h_{FEO}}$$

needed to drive the transistor to the saturation region $V_{CB} = 0$ V.

$$a = \frac{I_{B2}}{I_{B0}} = -\frac{h_{FEO} \times I_{B2}}{I_C}$$

Saturation (overdriving factor ü) is the ratio between the minimum value of the base current, I_{B1}, to the base current needed to drive the transistor to the saturation region $V_{CB} = 0$ V.

$$I_{B0} = \frac{I_C}{h_{FEO}}$$

$$ü = \frac{h_{FEO} \times I_{B1}}{I_C}$$

With a given saturation factor ü, on-off base current ratio, a, transistor type, on-state (τ) and storage (τ_S) time constants, the following conditions for switching characteristics are valid:

$$t_r \approx \tau \times \ln\left(\frac{ü-0.1}{ü-0.9}\right)$$

$$t_f \approx \tau \times \ln\left(\frac{a+0.9}{a+0.1}\right)$$

$$t_s \approx \tau_s \times \ln\left(\frac{a+ü}{a+1}\right)$$

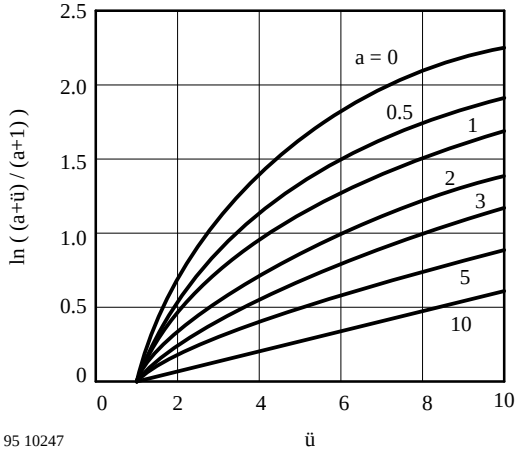


Figure 22.

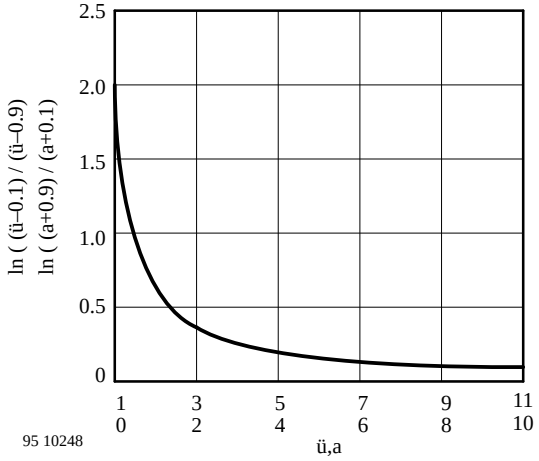


Figure 23.

Switching Characteristics of High Voltage Transistors

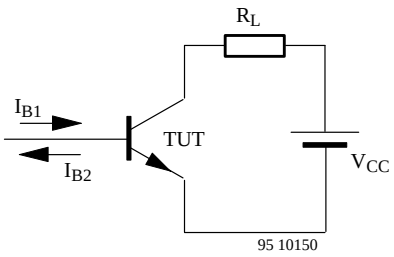


Figure 24. Basic circuit for resistive load

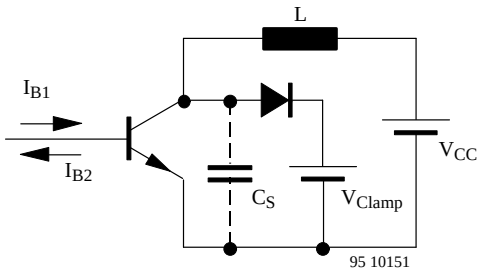


Figure 25. Basic circuit for inductive load

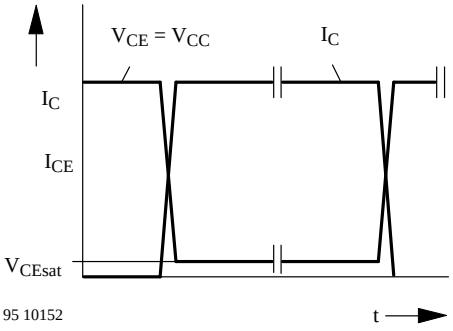


Figure 26. Typical current and voltage with resistive load

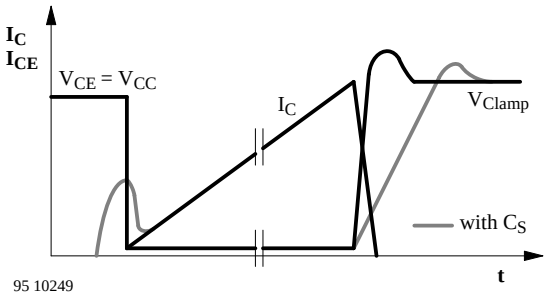


Figure 27. Typical current and voltage response with inductive load

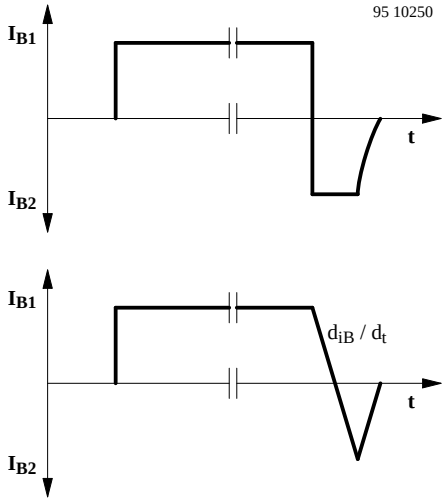


Figure 28. Typical driving conditions for resistive load and inductive load

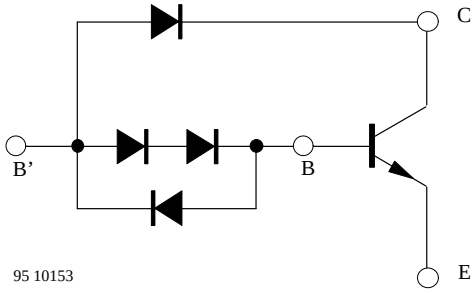


Figure 30. Anti-saturation circuitry (baker clamp)

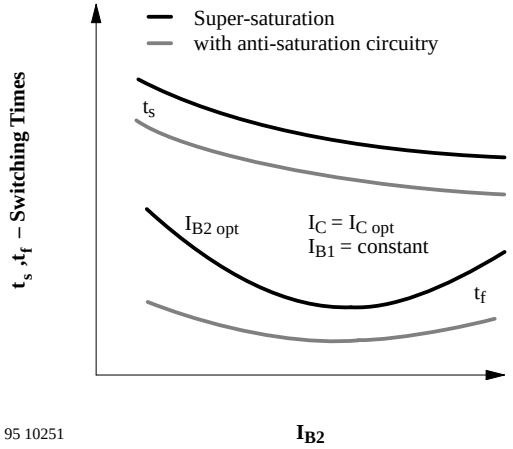


Figure 29. Typical switching responses at different driving conditions

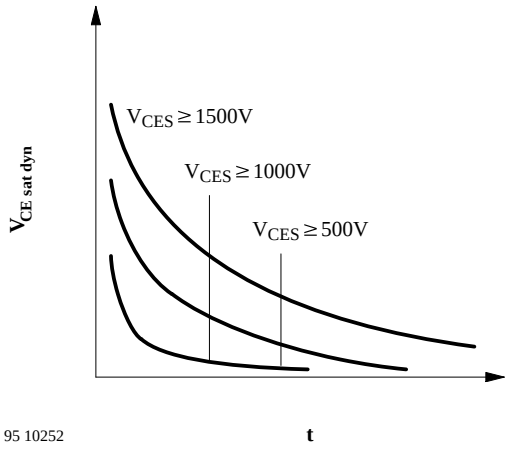


Figure 31. Typical switching-on response (dynamic saturation)

Mounting Instructions

General

Semiconductor devices can be mounted in any position. If the diameter of the terminal leads is less than 0.5 mm, bending of leads is allowed at least 1.5 mm away from the semiconductor body (header). Bending should be avoided if the thickness is greater than 0.5 mm. When semiconductor devices are mounted near those components with high heat generation, consideration should be given to high ambient temperature.

Soldering Instructions

Semiconductor devices should be protected against overheating due to soldering. It is recommended to keep the are kept as long as possible and to solder only at the end of the terminal. Otherwise, precautions should be taken for heat transfer.

The junction temperature of a semiconductor device may exceed the maximum absolute junction temperature for a short time (a maximum of one minute), such as 110°C for germanium and 200°C for silicon devices.

Table 3 shows the maximum soldering iron (or solder bath) temperatures are permissible.

Heat Removal

To maintain the thermal equilibrium, the heat generated in the semiconductor junction(s) must be removed to the ambient.

For low-power devices, the natural heat-conductive path between case and surrounding air is usually adequate for this purpose.

Finally, high-power devices require special heat sinks. The cooling effect can be increased further by the use of special coolants or air blowers.

The heat generated in the junction is conveyed to the case or header by conduction rather than convection. A measure of the effectiveness of heat conduction is the inner thermal resistance or thermal resistance junction-case, R_{thJC}, the value of which is governed by the construction of the device.

Any heat transfer from the case to the surrounding air involves radiation convection and conduction. The effectiveness of transfer expressed in terms of an R_{thCA} value, i.e., the external or case-ambient thermal resistance. The total thermal resistance junction ambient is consequently:

$$R_{thJA} = R_{thJC} + R_{thCA}$$

The total maximum power dissipation, $P_{tot\,max}$, of a semiconductor device can be expressed as follows:

$$P_{tot\,max} = \frac{T_{jmax} - T_{amb}}{R_{thJA}} = \frac{T_{jmax} - T_{amb}}{R_{thJC} + R_{thCA}}$$

where

T_{jmax}
maximum junction temperature

T_{amb}
highest ambient temperature likely to be reached under the most unfavorable conditions

Table 3.

	Iron Soldering			Dip or Flow Soldering		
	Iron Temperature	Soldering Distance from the Case	Max. Allowable Soldering Time	Soldering Temperature	Soldering Distance from the Case	Max. Allowable Soldering Time
Metal case	≤ 245°C	1.5 to 5 mm	5 s	≤ 245°C	> 1.5 mm	5 s
	≤ 245°C	> 5 mm	10 s			
	245 to 350°C	> 5 mm	5 s	245 to 300°C	> 5 mm	3 s
Plastic case	≤ 245°C	2 to 5 mm	3 s	≤ 245°C	> 2 mm	3 s
	≤ 245°C	> 5 mm	5 s	245 to 300°C	> 5 mm	2 s
23 A 3 DIN41869 (SOT 23)	≤ 250°C	–	10 s	≤ 250°C	–	10 s

R_{thJC}
thermal resistance, junction-case

R_{thJA}
thermal resistance, junction-ambient

R_{thCA}
thermal resistance, case-ambient (the value depends on cooling conditions)

If a heat dissipator or sink is used, R_{thCA} depends on the thermal contact between case and heat sink, heat propagation conditions in the sink, and the rate at which heat is transferred to the surrounding air.

Therefore, the maximum allowable total power dissipation for a given semiconductor device can be influenced only by changing T_{amb} and R_{thCA}. The value of R_{thCA} can be obtained either from the data of heat sink suppliers or through direct measurements.

When using cooling plates as heat sink without optimum performance, the following approach is acceptable.

The curves shown in figures 32 and 33 are given for thermal resistance, R_{thCA}, by using square plates of aluminium with edge length, a, but with different thicknesses. The device case should be mounted directly on the cooling plate.

The edge length, a, derived from figures 32 and 33 for a given R_{thCA} value must be multiplied with α and β:

$$a' = a \times \beta \times \alpha$$

where

α = 1.00 for vertical arrangement
α = 1.15 for horizontal arrangement
β = 1.00 for bright surface
β = 0.85 for dull black surface

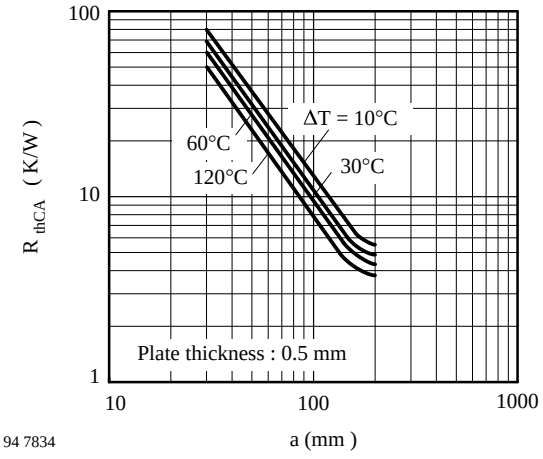


Figure 32.

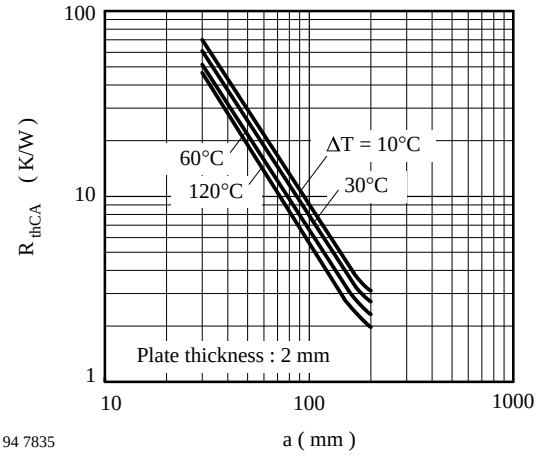


Figure 33.

Example

For a silicon power transistor with T_{jmax} = 150°C and R_{thJC} = 5 K/W, a 2 mm aluminium square sheet is used in a horizontal arrangement. The maximum ambient temperature is 50°C and the maximum power dissipation is $P_{tot\ max}$ = 8 W.
Calculate edge length of the square plate.

$$P_{tot\ max} = \frac{T_{jmax} - T_{amb}}{R_{thJC} + R_{thCA}}$$

$$R_{thCA} = \frac{T_{jmax} - T_{amb}}{P_{tot}} - R_{thJC} =$$

$$\frac{150°C–50°C}{8\ W} – 5°C/W = 7.5\ K/W$$

$\Delta T = T_{case} - T_{amb}$ can be calculated from

$$P_{tot\ max} = \frac{T_{jmax} - T_{amb}}{R_{thJC} + R_{thCA}} = \frac{T_{case} - T_{amb}}{R_{thCA}}$$

$$T_{case}–T_{amb} = \frac{R_{thCA}\ (T_{jmax}–T_{amb})}{R_{thJC} + R_{thCA}}$$

$$= \frac{7.5°C/W\ (150°C–50°C)}{5\ K/W + 7.5\ K/W} = 60°C$$

With R_{thCA} = 7.5 K/W and ΔT = 60°C, plate thickness = 2 mm. Therefore, the edge length a = 90 mm. This value should be multiplied with α = 1.15 due to horizontal arrangement.
Hence, the actual edge length = 105 mm.

For a given plate sheet length, the allowable power dissipation should be first calculated with a supposed ΔT. The result should be corrected then with the actual ΔT.

Maximum Operating Range for Power Transistors

To avoid the destruction of power transistors, certain maximum ratings must be observed. These ratings define a safe operating area, as shown in figure 34 for both steady and pulse state conditions. They are valid only for power transistors operating with thermal stability and a specified case temperature.

As shown in figure 34, the safe operating area is limited for forward operation conditions by the four maximum ratings explained below:

A Maximum steady collector current
By exceeding this value, there is a possibility of chip destruction or melting of the connecting wires inside the device.

B Maximum power dissipation due to thermal resistance, R_{thJC}, and junction temperature, T_{jmax}

For steady operation, the product $V_{CE} \times I_C$ is constant; therefore, the curve has a slope of 135°C in double logarithmic scale as shown in figure 34.

C Maximum rating against second breakdown
Is due to current concentration which results in hot spots, and therefore, localized melting of the crystal near or at the narrow base width, if the applied energy, i.e., voltage, current and time, exceeds a critical value. These hot spots occur either at the edges or in the middle of the base according to whether the emitter junction is forward or reverse biased.

The energy required for the second breakdown is considerably lower in the case of reverse-biased emitter junction (as compared to forward-biased emitter junction) because the current concentration takes place in a very small area.

The allowable power dissipation decreases with increasing voltage. Therefore, the slope of the corresponding curve is less than 135°C.

D Maximum steady collector voltage
By exceeding this value, there is a possibility of avalanche breakdown.

It is possible to extend the safe operating area (dotted curves) by pulse operation as shown in diagram. Even in this case the maximum allowable energy must lie within the specified value.

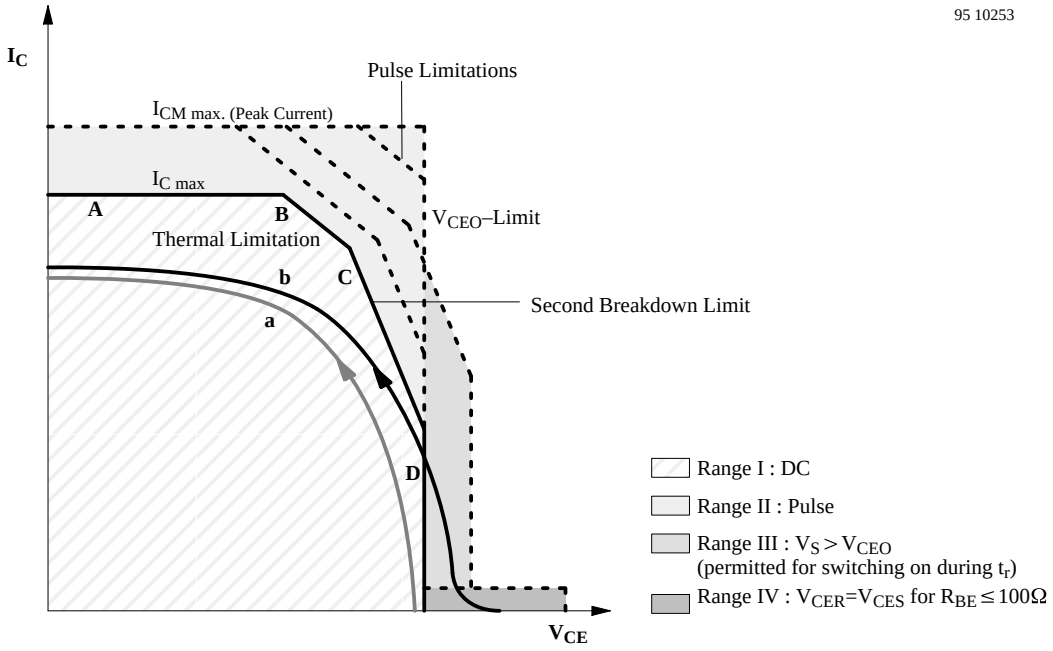


Figure 34. Safe operation area (SOA) with switch on curves

SOA Limitation for Switch-On Time

Figure 34 shows the SOA diagram and the switch-on curves (a and b) at resistive load and inductive load.

a) The transistor switches on when the collector voltage is smaller than V_{CEO}.

There is no danger for the transistor because the switch-on time is very short.

For this operation, the limitation of the SOA for

$t_{on} = 1\ \mu s$ and $\frac{t_{om}}{T} \leq \frac{1}{100}$ is valid.

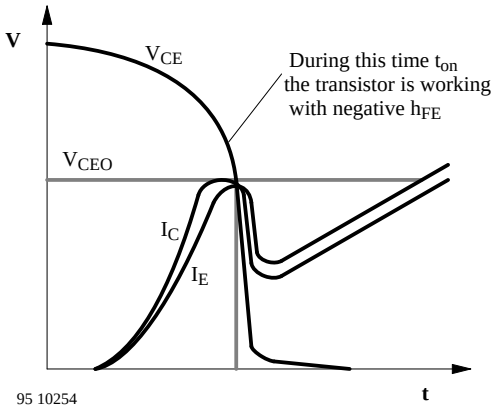


Figure 35. Range of negative current gain

b) The transistor switches on when the inductance in the collector circuit is not yet unloaded and the flyback voltage V_{CE} is higher than V_{CEO} of the transistor.

In this case, the transistor works with negative h_{FE}. These are the hardest working conditions for the transistor (figure 35).

SOA Limitation During Switch-Off Time

The usual SOA diagram if the forward-biased transistor is not valid the pulse capability is calculated during the collector current fall time because the transistor is switched off with reverse base current. In this case, the transistor works with negative h_{FE}.

At high-voltage power transistors, the SOA for the switch-off condition, base reverse biased, permits during the fall time, V_{CE}, higher than V_{CEO} of the transistor. As an example for a special 50 A, figure 36 shows the switch-off conditions in the case there is no reduced slope of the flyback voltage.

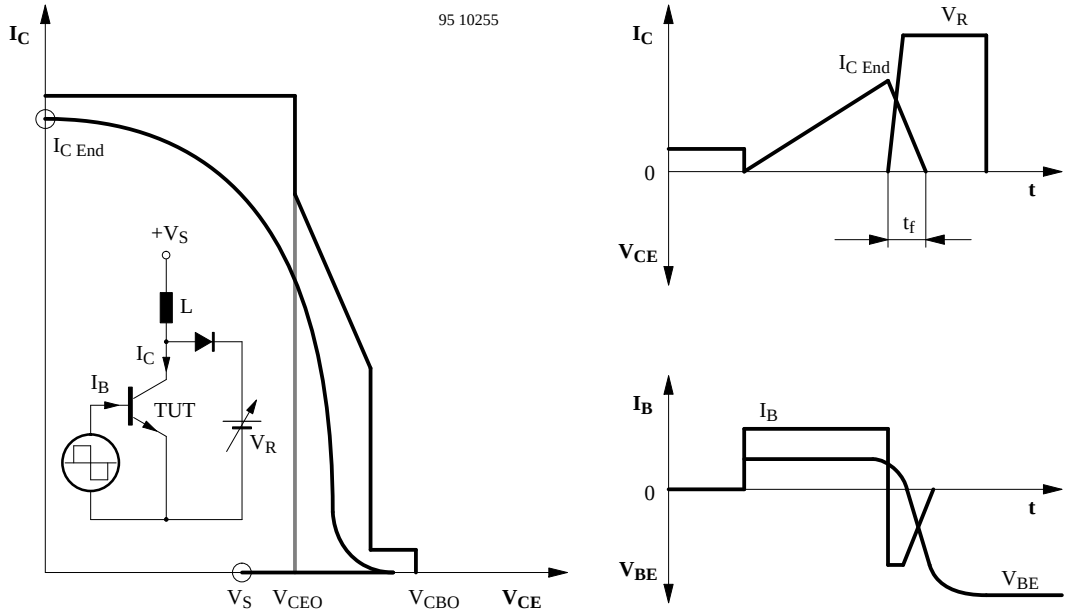


Figure 36. Reverse base safe operation area (RBSOA)

Operation When the Transistor Is Switched Off and $V_{flyback} > V_{CEO}$

Base driving conditions

An emitter-grounded switched-off transistor withstands voltages up to V_{CBO} as long as the base-emitter voltage cannot reach the threshold voltage. This is achieved in a device by a low BE resistance parallel to the BE diode or, even better, by a switch-off potential. By dimensioning the BE conditions for the switched-off transistor, the voltage drop produced by the maximum leakage current guaranteed for the maximum junction temperature is taken into account. The maximum leakage current, $I_{CBO,}$ for T_{jmax} is the current limitation of the SOA region for the switched-off transistor and for voltages between V_{CEO} and V_{CBO} (figure 36). In Telefunken's data sheets, it is guaranteed that the switched-off transistor with a resistance smaller than 100 W parallel to the BE diode and with no reverse base voltage withstands $V_{CE} = V_{CB}$ up to the maximum junction temperature when the limits of the figure 34 are respected.

These are the most disadvantageous switched-off conditions and are seldom encountered.

$V_{CEV} = V_{CBO}$ when the following condition is fulfilled:

$$V_{CBO} \text{ (at } T_{jmax}) \times R_{BE} - |V_{BE}| \leq 0.3 \text{ V}$$

Thermal stability

In unclamped flyback converters, the switched-off transistor normally has a collector voltage between it's V_{CBO} and V_{CBO}. It is a requirement that during this time the thermal stability of the leakage current is given. If the transistor reaches thermal instability, it will be damaged because of insufficient limitation of the increasing leakage current by the inductive load.

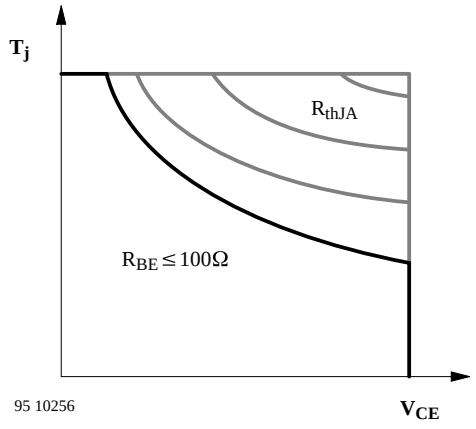


Figure 37. Range of guaranteed thermal stability

Thermal instability occurs when the input power, generated by the increasing leakage current at V_{CE}, is higher than the heat dissipation to the surroundings at the same time.

The maximum leakage current at the beginning of thermal instability can be calculated with the following formula:

$$I_{CBO} \text{ (at } T_{jmax}) = \frac{20 \text{ C}}{R_{th} \times V_{CE}}$$

R_{th} is the determination for the switch-off conditions. It is very important that transistors work with sufficient heat dissipaters.

Figure 37 shows the allowed maximum junction temperature of the transistor versus V_{CE} and guaranteed thermal stability. This figure is based on the maximum I_{CBO} at T_{jmax} and will be published for all Telefunken electronic high voltage transistors.

Quality Data

With an extensive system consisting of qualification, intermediate and final tests, Telefunken endeavours to supply the customers with components that fulfil the specifications of the OEM industry.

If you are interested in detailed informations regarding "TELEFUNKEN Quality Assurance of Semiconductor Components", please request four our brochure "TELEFUNKEN Quality and Reliability".

Delivery Quality

To secure the delivery quality, the following specifications are given:

- Maximum and minimum values of the characteristics
- AQL- (Acceptable Quality Level) values

Shipment lots whose defect percentage is equal to or less than the percentage given in AQL value shall be accepted with greater probability (L ≥ 90%) due to sampling tests (see the single sampling plan in chapter 'Sampling Inspection Plans').

Classification of Defects

The possible defects with which a semiconductor device can be subjected are classified according to the probable influence of existing circuits:

- Total (critical) defect

When one of these defects occurs, the functional use of the device is impossible.

Examples:
open contacts, inter-electrode short circuits, breakdown in reverse characteristics, wrong type designation, broken leads, critical case defects

- Major defect

A defect which is responsible for the failure of a device.

If the specified limits given in the datasheets are exceeded, it is considered as major defect. Typical values are given for orientation which are not tested.

- Minor defect

A defect which is responsible for the function of a device with no or only a slight reduction in effectiveness

There could be external defects such as wrong marking or light scratches.

AQL Values

According to the classification of defects mentioned in the chapter before, the following AQL values, are valid for data sheets of semiconductor devices for professional equipments and applications unless otherwise specified. Inspection follows the single sampling plan for attribute testing, AEG 1415 (see chapter 'Sampling inspection plans'), which corresponds mainly to DIN 40080 or MIL-STD-105 D inspection level II.

A cumulative AQL value equal to 0.4% is valid for all defects mentioned above.

Sampling Inspection Plans

Lists of symbols:

AQL	Acceptable Quality Level
N	Lot size
n	Sample size
c	Acceptance number
D_{max}	Average outgoing quality level

Table 4. Single sampling plan for attribute testing (according to DIN)

<table>
<tr><td rowspan="2">Normal Inspection</td><td colspan="11">AQL</td><td rowspan="2">Reduced Inspection</td></tr>
<tr><td>0.06</td><td>0.10</td><td>0.15</td><td>0.25</td><td>0.40</td><td>0.65</td><td>1.0</td><td>1.5</td><td>2.5</td><td>4.0</td><td>6.5</td></tr>
<tr><td>N</td><td colspan="11">n–c
(D_{max} in %)</td><td>N</td></tr>
<tr><td>2–15</td><td rowspan="10">200–0
(0.18)</td><td rowspan="9">125–0
(0.29)</td><td rowspan="7">80–0
(0.45)</td><td rowspan="5">50–0
(0.71)</td><td rowspan="4">32–0
(1.1)</td><td rowspan="3">20–0
(1.7)</td><td rowspan="2">13–0
(2.6)</td><td rowspan="2">8–0
(3.9)</td><td rowspan="2">5–0
(6.7)</td><td>3–0
(9.6)</td><td>2–0
(15.6)</td><td>2–15</td></tr>
<tr><td>16–50</td><td>13–1
(4.8)</td><td>8–1
(9.2)</td><td>16–150</td></tr>
<tr><td>51–150</td><td rowspan="2">32–1
(2.3)</td><td>20–1
(3.6)</td><td>20–2
(6.0)</td><td>20–3
(8.4)</td><td>151–280</td></tr>
<tr><td>151–280</td><td rowspan="2">50–1
(1.5)</td><td>32–2
(3.8)</td><td>32–3
(5.4)</td><td>32–5
(8.8)</td><td>281–500</td></tr>
<tr><td>281–500</td><td rowspan="2">80–1
(1.0)</td><td>50–2
(2.4)</td><td>50–3
(3.5)</td><td>50–5
(5.7)</td><td>50–7
(8.1)</td><td>501–1200</td></tr>
<tr><td>501–1200</td><td rowspan="2">125–1
(0.64)</td><td>80–2
(1.6)</td><td>80–3
(2.2)</td><td>80–5
(3.7)</td><td>80–7
(5.2)</td><td>80–10
(7.7)</td><td>1201–3200</td></tr>
<tr><td>1201–3200</td><td rowspan="3">200–1
(0.41)</td><td>125–2
(1.1)</td><td>125–3
(1.5)</td><td>125–5
(2.4)</td><td>125–7
(3.5)</td><td>125–10
(5.0)</td><td>125–14
(7.2)</td><td>3201–10000</td></tr>
<tr><td>2101–10000</td><td rowspan="2">315–1
(0.27)</td><td>200–2
(0.68)</td><td>200–3
(0.68)</td><td>200–5
(1.6)</td><td>200–7
(2.2)</td><td>200–10
(3.2)</td><td>200–14
(4.6)</td><td rowspan="2">200–21
(7.3)</td><td>10001–35000</td></tr>
<tr><td>10001–35000</td><td>500–1
(0.17)</td><td>315–2
(0.44)</td><td>315–3
(0.61)</td><td>315–5
(0.99)</td><td>315–7
(1.4)</td><td>315–10
(2.1)</td><td>315–14
(3.0)</td><td>315–21
(4.7)</td><td></td></tr>
</table>

Table 5. Single sampling plan for destructive or very costly test procedures (AEG 1416, Z-plans)

Normal Inspection	AQL											Reduced Inspection
	0.06	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	
N	n–c (D_{max} in %)											N
2–25	200–0 (0.18)	125–0 (0.29)	80–0 (0.46)	50–0 (0.74)	32–0 (1.2)	20–0 (1.8)	13–0 (2.8)	8–0 (4.5)	5–0 (7.2)	3–0 (11.6)	2–0 (16.6)	2–50
26–90											8–1 (10.8)	51–150
91–150										13–1 (6.3)		151–500
151–500									20–1 (4.1)			501–3200
501–1200								32–1 (2.6)		20–2 (6.8)	20–3 (9.5)	3201–35000
1201–10000							50–1 (1.7)		32–2 (4.3)	32–3 (6.1)	32–5 (9.9)	
10001–35000						80–1 (1.1)		50–2 (2.7)	50–3 (3.9)	50–5 (6.3)	50–7 (9.0)	

Data Sheet Construction

Data sheet information is generally presented in the following sequence:

- Device description
- Dimensions (mechanical data)
- Absolute maximum ratings
- Thermal data – thermal resistances
- Electrical characteristics

Additional information on device performance is provided if necessary.

Device Description

The following information is provided: part number, semiconductor materials used, sequence of zones, technology used, device type and, if necessary, construction.

Information on typical applications and special features is also given.

Dimensions (Mechanical Data)

The mechanical data include important dimensions and the sequence of connections supplemented by a circuit diagram. Case outline drawings carry DIN, JEDEC or commercial designations. Information on weight is also given.

Note:

If the dimensional information does not include any tolerances, then the lead length and mounting hole dimensions are minimum values. All other dimensions are maximum.

Absolute Maximum Ratings

The absolute maximum ratings indicate the maximum permissible operational and environmental conditions. Exceeding any of these conditions could result in the destruction of the device. Unless otherwise specified, an ambient temperature of 25 ± 3°C is assumed for all absolute maximum ratings. Most absolute ratings are static characteristics; if they are measured by a pulse method, then the associated measurement conditions are stated.
Maximum ratings are absolute (i.e., not interdependent). Any equipment incorporating semiconductor devices must be designed so that even under the most unfavorable operating conditions, the specified maximum ratings of the devices used are never exceeded. These ratings could be exceeded because of changes in

- supply voltage
- the properties of other components used in the equipment
- control settings
- load conditions
- drive level
- environmental conditions
- the properties of the devices themselves (aging)

Thermal Data – Thermal Resistances

As some thermal data (e.g., junction temperature, storage temperature range, total power dissipation), impose a limit on the application range of the device, they are given in the chapter ‘Absolute maximum ratings’. A special section is provided for thermal resistances. The thermal resistance, junction-ambient (R_{thJA}) quoted, is measured without artificial cooling, i.e., under the worst conditions.

Temperature coefficients are listed together with the associated parameters in the chapter ‘Switching Characteristics’.

Characteristics

Under this heading the most important operational electrical characteristics (minimum, typical and maximum values) are grouped together with associated test conditions supplemented with curves.

Electrical characteristics

The distinctive feature of semiconductor devices is that they are characterised with electrical characteristics which contain static (dc), dynamic (ac), two-port characteristics and family of curves.

Static (dc) characteristics

DC characteristics explain the dc properties of a semiconductor device. They are temperature dependent and are valid only for a given ambient or case temperature.

Dynamic (ac) characteristics

AC characteristics explain the ac or pulse properties of a semiconductor device. According to type they are given the important AF, HF or switching characteristics. The dynamic (ac) characteristics are valid only under special operating conditions. If necessary, they are supplied with corresponding measuring circuits.

Family of curves

Besides the static (dc) and dynamic (ac) characteristics, a family of curves are given for specified operating conditions. They show the typical interdependence of individual characteristics. Scattering limits are also given. These signify that at least 95% of delivered devices lie inside these tolerances.

Additional Informations

Preliminary specifications

This heading indicates that some information on the device concerned may be subject to slight changes.

Not for new developments

This heading indicates that the device concerned should not be used in equipment under development. It is, however, available for present production.